TRANSMITTAL OF APPEAL BRIEF	Docket No. 108298743US

In re Application of: Benson et al.

Application No.	Filing Date	Examiner	Group Art Unit
10/713,626-Conf. #2439	November 13, 2003	J. M. Im	2811

Invention: MICROELECTRONIC DEVICES HAVING CONDUCTIVE COMPLEMENTARY STRUCTURES AND METHODS OF MANUFACTURING MICROELECTRONIC DEVICES HAVING CONDUCTIVE COMPLEMENTARY STRUCTURES

TO THE COMMISSIONER OF PATENTS:

Transmitted herewith is the Appeal Brief in this application, with respect to the Notice of Appeal filed: December 26, 2006 .

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[X] Large Entity [ ] Small Entity

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Dated: April 26, 2007

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(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Benson et al.

Application No.: 10/713,626 Confirmation No.: 2439

Filed: November 13, 2003 Art Unit: 2811

For: MICROELECTRONIC DEVICES HAVING CONDUCTIVE COMPLEMENTARY STRUCTURES AND METHODS OF MANUFACTURING MICROELECTRONIC DEVICES HAVING CONDUCTIVE COMPLEMENTARY STRUCTURES

Examiner: J. M. Im

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This brief is filed in furtherance of the Notice of Appeal filed December 26, 2006.

The fees required under § 41.20(b)(2) are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF. A separate Petition for Extension of Time and the requisite fees are filed concurrently herewith.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

I. Real Party In Interest
II Related Appeals and Interferences
III. Status of Claims
IV. Status of Amendments

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is Micron Technology, Inc.

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 15 claims pending in application.

B. Current Status of Claims

1. Claims canceled: 33 and 35-59
2. Claims withdrawn from consideration but not canceled: 1-8, 18, 25-32, and 34
3. Claims pending: 9-17 and 19-24
4. Claims allowed: none
5. Claims rejected: 9-17 and 19-24

C. Claims On Appeal

The claims on appeal are claims 9-17 and 19-24.

IV. STATUS OF AMENDMENTS

No claims have been added, amended, or canceled after the issuance of the Final Office Action mailed July 26, 2006.

V. SUMMARY OF CLAIMED SUBJECT MATTER

To meet the ever increasing demand for smaller electronic products, there is a continued drive to reduce the height and the surface area or the "footprint" of packaged microelectronic devices. (*See e.g.*, Specification, 3:5-8). One technique for increasing the density of microelectronic devices is to stack one device on top of another in a wire-bonded, stacked-die arrangement, as illustrated in Figure 1 (reproduced below). (*See e.g.*, Specification, 1:11-13).

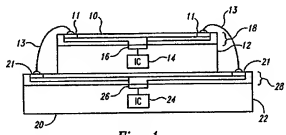

Fig. 1

As shown in Figure 1, a first microelectronic device 10 is stacked on top of a second microelectronic device 20. (*See e.g.*, Specification, 1:12-14). The first microelectronic device 10 includes a die 12 having an integrated circuit 14 and a plurality of bond-pads 16 electrically coupled to the integrated circuit 14. (*See e.g.*, Specification, 1:14-16). The first microelectronic device 10 further includes a redistribution layer 18 having a plurality of first pads 11 electrically coupled to corresponding bond-pads 16. (*See e.g.*, Specification, 1:16-18). The second microelectronic device 20 similarly includes a die 22 having an integrated circuit 24 and a plurality of bond-pads 26 electrically coupled to the integrated circuit 24. (*See e.g.*, Specification, 1:16-18). The second microelectronic device 20 further includes a redistribution layer 28 having a plurality of second pads 21 electrically coupled to corresponding bond-pads 26. (*See e.g.*, Specification, 1:18-20). A

plurality of wire-bonds 13 extend between first pads 11 and second pads 21 to electrically couple the first and second devices. (*See e.g.*, Specification, 1:22-24).

One drawback of this arrangement is that forming wire-bonds for high-density, fine-pitch arrays of high performance devices may not be feasible because wire-bonding can be a complex and expensive process. (*See e.g.*, Specification, 1:27-29). Moreover, positioning the second pads 21 outside of the first microelectronic device 10 to accommodate the wire-bonds 13 undesirably increases the footprint of the stacked-die arrangement. (*See e.g.*, Specification, 1:29-31).

A. Claim 9

Several embodiments of the present invention resolve the above-described drawback by providing conductive mating structures on individual microfeature workpieces. (*See e.g.*, Specification, 7:17-19). For example, one embodiment of a microfeature workpiece 200 having such conductive mating structures is illustrated in Figure 3 (reproduced below).

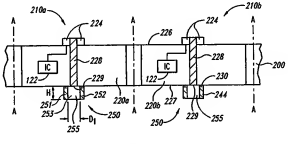

Fig. 3

As shown in Figure 3, the microfeature workpiece includes a plurality of first dies 220a-b individually having a first integrated circuit 122 and a plurality of first pads 224 electrically coupled to the first integrated circuit 122. As explained below, the first dies 220a-b are configured to be stacked on second dies (*See e.g.*, Specification, 9:16-24). The first dies 220a-b can have a plurality of first conductive mating structures 250 electrically coupled to the first pads 224 for stacking the first dies 220a-b on the second dies. (*See e.g.*, Specification, 9:16-21). The first conductive mating structures 250 project away from the first dies 220a-b and have openings 255 configured to receive

and interconnect with corresponding complementary second conductive mating structures on second dies.

One example of a microfeature workpiece 110 having a plurality of second dies 120 on which the first dies 220a-b can be mounted is illustrated in Figure 2C (reproduced below). Individual second dies 120 include a conductive mating structure 150 coupled to and projecting from corresponding bond-pads 124 and optional seed layers 130. (*See e.g.*, Specification, 8:21-29).

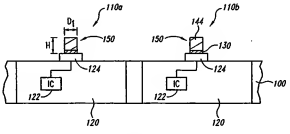

Fig. 2C

Figure 4A (reproduced below) illustrates the microelectronic devices 210 of Figure 3 stacked on top of the corresponding microelectronic devices 110 of Figure 2C.

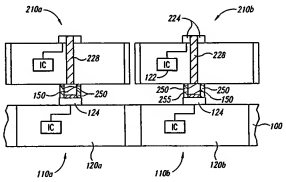

Fig. 4A

Several embodiments of the mating structures can properly align the stacked lower and upper microelectronic devices 110 and 210. The conductive mating structures, moreover, combine the stacking and aligning processes into one step to simplify the stacking procedure. The first and

second conductive mating structures 150 and 250 can also fix the distance between the microelectronic devices 110 and 210.

B. Claim 21

In another embodiment, as set forth in claim 21, a microelectronic die includes an integrated circuit, a plurality of bond-pads electrically coupled to the integrated circuit, and a plurality of first conductive mating structures on corresponding bond-pads. (*See e.g.*, Specification, 9:16-24). The first conductive mating structures project away from the die directly from corresponding bond-pads and have openings configured to receive and interface with corresponding second conductive mating structures on another microelectronic device to which the die is to be mounted. Id.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 9-17 and 19-24 were rejected under 35 U.S.C. § 103(a) over the combination of U.S. Patent No. 6,608,371 to Kurashima et al. ("Kurashima") and U.S. Patent No. 6,525,413 to Cloud et al. ("Cloud").

VII. ARGUMENT

Claims 9-17 and 19-24 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kurashima in view of Cloud. "[T]he examiner bears the initial burden of presenting a *prima facie* case of obviousness." *In re Rijckaert*, 9 F.3d 1531, 1532, 28 USPQ2d, 1955, 1956 (Fed. Cir. 1993). To establish a *prima facie* case of obviousness, the Examiner needs to (a) identity prior art references that disclose all the elements of the claims, and (b) provide a suggestion to combine the references. (M.P.E.P. § 2143.) As set forth in detail below, the Examiner has failed to satisfy the burden of presenting a *prima facie* case of obviousness because (1) even if combined, the combined teachings of Kurashima and Cloud still do not teach or suggest all the limitations of the pending claims; and (2) one of ordinary skill in the art would not modify Kurashima's teachings as suggested by the Examiner because, among other reasons, such modification may render Kurashima's device unsatisfactory for its intended purpose.

A. Grouping of Claims

Appellant believes that the following groups of claims 9-17 and 19-24 are separately patentable. Claims 9-17 and 19-24 do not stand or fall together with respect to the rejection under 35 U.S.C. § 103(a), but instead are grouped together as follows:

Group I: Claims 9-17, 19, and 20

Group II: Claims 21-24

Group I consists of claims 9-17, 19, and 20. Claims 9-17, 19, and 20 recite a microfeature workpiece having a plurality of first conductive mating structures projecting away from the first dies and having openings configured to receive and interconnect with corresponding complementary second conductive mating structures on second dies which are to be mounted to corresponding first dies. As claims 9-17, 19, and 20 recite a microfeature workpiece distinctive from the other claims, Group I properly states a separately patentable claim group.

Group II consists of claims 21-24. Claims 21-24 recite a microelectronic die having an integrated circuit, a plurality of bond-pads electrically coupled to the integrated circuit, and a plurality of first conductive mating structures projecting away from the die directly from corresponding bond-pads. As claims 21-24 recite a microelectronic die distinctive from the other claims, Group II properly states a separately patentable claim group.

B. Patentability of Group I – Claims 9-17, 19, and 20

Claim 9 is directed to a microfeature workpiece including a plurality of first dies and a plurality of first conductive mating structures on the first dies. The individual first dies have a first integrated circuit and a plurality of first pads electrically coupled to the first integrated circuit. The first conductive mating structures are positioned at least proximate to the first pads and project away from the first dies. The first conductive mating structures have openings configured to receive and interconnect with corresponding complementary second conductive mating structures on second dies.

Kurashima discloses several embodiments of a method for manufacturing a semiconductor device. (Abstract). One particular embodiment is described with reference to Figures 1A-2B (reproduced below). As illustrated in Figure 1A, the semiconductor device initially includes a chip 10 formed in a semiconductor wafer 12. (column 6, lines 16-20). The chip 10 includes a plurality of electrodes 14 and plating 16 on top of each of the electrodes 14. (column 6, lines 23-25).

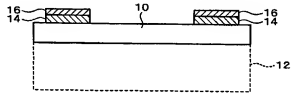

Figure 1A

Kurashima discloses forming a first through hole 18 in the chip 10. (column 6, lines 55-57). Each of the first through holes 18 penetrates through the chip 10 at the location of each electrode 14, as illustrated in Figure 1B. (column 6, lines 57-59).

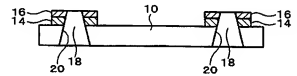

Figure 1B

An insulating material 22 is then deposited to fill the first through holes 18, as illustrated in Figure 1C. (column 7, lines 43-47). The insulating material 22 can fill the first through hole 18 to reliably insulate the semiconductor chip 10 from the first through hole 18.

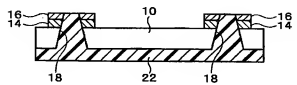

Figure 1C

Second through holes 24 are then formed in the insulating material 22. The second through hole 24 have a diameter that is smaller than that of the first through holes 18. (column 8, lines 32-35). A conductive member 28 is then deposited to fill the second through hole 24, as illustrated in Figure 2B. (column 8, lines 65-67). The insulating material 22 insulates the chip 10 from the conductive member 28. (column 9, lines 3-7).

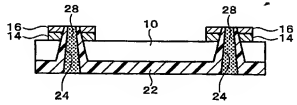

Figure 2B

A plurality of chips having the configuration as shown in Figure 2B can then be stacked and electrically connected with a solder 30, as illustrated in Figure 2C. (column 10, lines 23-30).

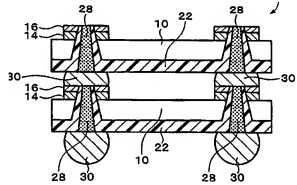

Figure 2C

In a second embodiment, Kurashima discloses preparing a first chip 11 that includes bumps 32 and a second chip 13 that includes the second through holes 24. (column 12, lines 32-42). The second through holes 24 in the second chip 13 are not filled with the conductive material 28. When the first and second chips 11, 13 are stacked, the bumps 32 penetrate the second through holes 24 of the second chip 13, as illustrated in Figure 4A (reproduced below). (column 13, lines 17-20). After

the bumps 32 are fitted into the second through holes 24, the bumps 32 can be melted in a reflow process. (column 13, lines 28-30).

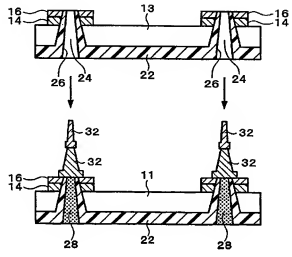

Figure 4A

Cloud discloses a package including a first die 10 and a second die 20, as illustrated in Figure 3 (reproduced below). (column 6, lines 19-21, 45-47).

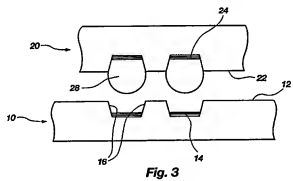

Fig. 3

The first die 10 includes an active surface 12, a plurality of recesses in the active surface 12, and a plurality of bond pads 14 exposed by corresponding recesses. (column 6, lines 22-26). The second die 20 includes an active surface 22, a plurality of bond pads 24, and a plurality of conductive structures 28 on corresponding bond pads 24 that project from the active surface 22. (column 6, lines 47-55). The second die 20 is attached to the first die 10 by placing the conductive structures 28 in corresponding recesses of the first die 10. (column 7, lines 5-15).

The combined teachings of Kurashima and Cloud fail to teach or suggest several features of claim 9. For example, the combination of these references does not teach or suggest a microfeature workpiece including, *inter alia*, a plurality of "first conductive mating structures projecting away from the first dies and having openings configured to receive and interconnect with corresponding complementary second conductive mating structures on second dies" of claim 9. In the Final Office Action mailed July 26, 2006, the Examiner alleged that Kurashima's second through holes 24 correspond to "a plurality of first conductive mating structures" of claim 9. (Office Action, July 26, 2006, page 2). Kurashima's second through holes 24, however, are voids through the insulating material 22 that electrically isolates the conductive member 28 from the chip 10. The second through holes 24 are accordingly dielectric instead of being conductive. In the Advisory Action mailed November 28, 2006, the Examiner responds to this argument by alleging that Kurashima's conductive material 28 in the second through holes 24 makes the second through holes 24 conductive. (Advisory Action, Nov. 28, 2006, page 2). This statement is incorrect because the "hole" does not change, but rather the material that fills the hole is conductive. Moreover, in this embodiment of Kurashima, the conductive material 28 completely fills the second through holes 24 such that there is no conductive structure that has an opening in Kurashima. As a result, there is no "conductive mating structure" with "openings configured to receive corresponding complementary second mating structures" in Kurashima. Kurashima's second through holes 24 also do not project away from the semiconductor dies because the second through holes 24 do not extend beyond the edge of the semiconductor dies. Accordingly, neither embodiment of Kurashima discloses or suggests mating structures that are (1) conductive, (2) project away from the first dies, and (3) have an opening to receive corresponding complementary second mating structures.

Cloud also fails to disclose or suggest such a combination. For example, assuming, for the sake of argument, that Cloud's conductive structure 28 corresponds at least in part to the first mating structures of claim 9, Cloud's conductive structure 28 does not have "openings configured to receive corresponding complementary second mating structures." Instead, the conductive structure 28 are configured to be placed in a plurality of recesses in a semiconductor die. Moreover, assuming, that Cloud's recesses having the bond pads 14 correspond at least in part to the first mating structures of

claim 9, the recesses do not project away from the semiconductor die. Accordingly, Cloud fails to fill the void left by Kurashima. Therefore, the combined teachings of Kurashima and Cloud fail to teach or suggest all the features of claim 9.

Moreover, a person skilled in the art would not modify Kurashima's device to have the conductive mating structures with openings of claim 9 because Kurashima teaches away from replacing the insulating material 22 with a conductive material. Kurashima discloses that the insulating material 22 "insulate[s] the semiconductor chip 10 reliably within the first through holes 18." (Kurashima, 7:47-48.) If Kurashima's insulating material were replaced with conductive material, Kurashima's chip 10 would not be electrically insulated from the conductive material 28 in the second through holes 24 and short circuiting could occur. As a result, such modification may render Kurashima's device unsatisfactory for its intended purpose. Accordingly, one skilled in the art would not modify Kurashima's device to have a conductive material instead of the insulating material 22 as suggested by the Examiner.

Accordingly, the current rejection of claim 9 does not comply with Section 103(a) because (1) even if combined, the combined teachings of Kurashima and Cloud still do not teach or suggest all the features of the pending claims; and (2) one of ordinary skill in the art would not modify Kurashima's teachings as suggested by the Examiner because such a modification would result in an inoperable device. Therefore, the Section 103(a) rejection of claim 9 is improper and should be reversed. Claims 10-17, 19, and 20 depend from claim 9. Accordingly, the Section 103(a) rejection of claims 10-17, 19, and 20 is improper and should be reversed for at least the reasons discussed above with reference to claim 9 and for the additional features of these claims.

C. Patentability of Group II – Claims 21-24

Claim 21 is directed to a microelectronic die includes an integrated circuit, a plurality of bond-pads electrically coupled to the integrated circuit, and a plurality of first conductive mating structures on corresponding bond-pads. The first conductive mating structures project away from the die directly from corresponding bond-pads and have openings configured to receive and

interface with corresponding second conductive mating structures on another microelectronic device to which the die is to be mounted.

Even if Kurashima is combined with Cloud, the combined teachings of these references still do not teach or suggest all the limitations of claim 21, and one of ordinary skill in the art would not modify Kurashima's teachings as suggested by the Examiner, as described above with reference to Group I. For example, the combination of Kurashima and Cloud fails to disclose or suggest conductive mating structures with openings. This combination of references also fails to disclose or suggest that such mating structures project away from the die directly from the bond pads. In both Kurashima and Cloud, the conductive features projecting away from bond pads are solid without openings. Moreover, a person skilled in the art would not modify the conductive features in Kurashima and Cloud to have openings because the resulting electrical connections may have voids. Accordingly, the Section 103(a) rejection of claim 21 is improper and should be reversed for at least the reasons discussed above. Claims 22-24 depend from claim 21. Accordingly, the Section 103(a) rejection of claims 22-24 is improper and should be reversed for at least the reasons discussed above with reference to claim 21 and for the additional features of these claims.

The Commissioner is hereby authorized to charge any underpayment of fees to Deposit Account No. 50-0665 under Order No. 108298743US, from which the undersigned representative is authorized to draw.

Dated: 4/26/07

Respectfully submitted,

By _____
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VIII. CLAIMS APPENDIX

Claims Involved in the Appeal of Application Serial No. 10/713,626

1. (Withdrawn) A set of microfeature workpieces, the set comprising:

a first microfeature workpiece including a plurality of first microelectronic dies, wherein individual first dies have a first integrated circuit, a plurality of first pads electrically coupled to the first integrated circuit, and a plurality of first conductive complementary structures on corresponding first pads; and

a second microfeature workpiece including a plurality of second microelectronic dies, wherein individual second dies have a second integrated circuit, a plurality of second pads electrically coupled to the second integrated circuit, and a plurality of second conductive complementary structures on or at least proximate to corresponding second pads, the second conductive complementary structures projecting away from the second dies and having openings configured to receive and interface with the first conductive complementary structures.

2. (Withdrawn) The set of microfeature workpieces of claim 1 wherein the first conductive complementary structures include an aperture configured to receive at least a portion of one of the second conductive complementary structures.

3. (Withdrawn) The set of microfeature workpieces of claim 1 wherein the first conductive complementary structures have male configurations and the second conductive complementary structures have female configurations.

4. (Withdrawn) The set of microfeature workpieces of claim 1 wherein the first complementary structures have a generally triangular, circular, or rectangular configuration.

5. (Withdrawn) The set of microfeature workpieces of claim 1 wherein the first and second complementary structures comprise solder.

6. (Withdrawn) The set of microfeature workpieces of claim 1 wherein:

the first microelectronic dies include a first side and a second side opposite the first side;

the first pads comprise a plurality of first bond-pads on and/or in the first side of the first microelectronic dies;

the first conductive complementary structures are coupled to corresponding first bond-pads on the first side of the first microelectronic dies;

the second microelectronic dies include a first side and a second side opposite the first side;

the second pads comprise a plurality of second bond-pads on and/or in the first side of the second microelectronic dies; and

the second conductive complementary structures are coupled to corresponding second bond-pads on the first side of the second microelectronic dies.

7. (Withdrawn) The set of microfeature workpieces of claim 1 wherein:

the first microelectronic dies include a first side, a second side opposite the first side, a first bond-pad on and/or in the first side, and a conductive link extending from the first side to the second side;

the conductive links have a plurality of ends defining the first pads on the second side of the first microelectronic dies;

the first conductive complementary structures are coupled to the first pads on the second side of the first microelectronic dies;

the second microelectronic dies include a first side and a second side opposite the first side;

the second pads comprise a plurality of second bond-pads on and/or in the first side of the second microelectronic dies; and

the second conductive complementary structures are coupled to the second bond-pads on the first side of the second microelectronic dies.

8. (Withdrawn) The set of microfeature workpieces of claim 1 wherein:

the first microelectronic dies include a third die;

the first pads include a third pad and a fourth pad adjacent to the third pad on the third die; and

the first conductive complementary structures on the third and fourth pads are spaced apart from each other by a distance of less than approximately 100 microns.

9. (Previously presented) A microfeature workpiece, comprising:

a plurality of first dies, wherein individual first dies have a first integrated circuit and a plurality of first pads electrically coupled to the first integrated circuit; and

a plurality of first conductive mating structures at least proximate to the first pads, the first conductive mating structures projecting away from the first dies and having openings configured to receive and interconnect with corresponding complementary second conductive mating structures on second dies which are to be mounted to corresponding first dies.

10. (Original) The microfeature workpiece of claim 9 wherein the first conductive mating structures have generally circular configurations.

11. (Original) The microfeature workpiece of claim 9 wherein the first conductive mating structures have generally triangular configurations.

12. (Original) The microfeature workpiece of claim 9 wherein the first conductive mating structures have generally rectangular configurations.

13. (Original) The microfeature workpiece of claim 9 wherein the first conductive mating structures include an aperture configured to receive at least a portion of one of the second conductive mating structures.

14. (Original) The microfeature workpiece of claim 9 wherein the first conductive mating structures have male configurations.

15. (Original) The microfeature workpiece of claim 9 wherein the first conductive mating structures have female configurations.

16. (Original) The microfeature workpiece of claim 9 wherein the first conductive mating structures comprise solder.

17. (Original) The microfeature workpiece of claim 9 wherein:

the first dies include a first side and a second side opposite the first side;

the first pads comprise a plurality of bond-pads on and/or in the first side of the first dies; and

the first conductive mating structures are coupled to the bond-pads on the first side of the first dies.

18. (Withdrawn) The microfeature workpiece of claim 9 wherein:

the first dies include a first side, a second side opposite the first side, a bond-pad on and/or in the first side, and a conductive link extending from the first side to the second side;

the conductive links have a plurality of ends defining the first pads on the second side of the first dies; and

the first conductive mating structures are coupled to the first pads on the second side of the first dies.

19. (Original) The microfeature workpiece of claim 9 wherein:

the first dies include a third die;

the first pads include a second pad and a third pad adjacent to the second pad on the third die; and

the first conductive mating structures on the second and third pads are spaced apart from each other by a distance of less than approximately 100 microns.

20. (Original) The microfeature workpiece of claim 9 wherein the first conductive mating structures are formed on corresponding first pads.

21. (Previously presented) A microelectronic die, comprising an integrated circuit, a plurality of bond-pads electrically coupled to the integrated circuit, and a plurality of first conductive mating structures on corresponding bond-pads, the first conductive mating structures projecting away from the die directly from corresponding bond-pads and having openings configured to receive and interface with corresponding second conductive mating structures on another microelectronic device to which the die is to be mounted.

22. (Original) The microelectronic die of claim 21 wherein the first conductive mating structures have generally circular, triangular, or rectangular configurations.

23. (Original) The microelectronic die of claim 21 wherein the first conductive mating structures include an aperture configured to receive at least a portion of one of the second conductive mating structures.

24. (Original) The microelectronic die of claim 21 wherein the first conductive mating structures have a male or female configuration.

25. (Withdrawn) A set of stacked microelectronic devices, the set comprising:

a first microelectronic device including an integrated circuit, a plurality of first pads electrically coupled to the integrated circuit, and a plurality of first conductive mating structures at least proximate to corresponding first pads; and

a second microelectronic device including a plurality of second pads and a plurality of second conductive mating structures at least proximate to corresponding second

pads, wherein the second conductive mating structures project away from the second microelectronic device and have openings configured to receive and mate with corresponding first conductive mating structures of the first microelectronic device.

26. (Withdrawn) The set of stacked microelectronic devices of claim 25 wherein the first conductive mating structures include an aperture configured to receive at least a portion of the corresponding second conductive mating structure.

27. (Withdrawn) The set of stacked microelectronic devices of claim 25 wherein the first conductive mating structures have a male configuration and the second conductive mating structures have a female configuration.

28. (Withdrawn) The set of stacked microelectronic devices of claim 25 wherein the first conductive mating structures have a generally triangular, circular, or rectangular configuration.

29. (Withdrawn) The set of stacked microelectronic devices of claim 25 wherein:

the first microelectronic device includes a first side and a second side opposite the first side;

the first pads comprise a plurality of first bond-pads on and/or in the first side of the first microelectronic device;

the first conductive mating structures are coupled to corresponding first bond-pads on the first side of the first microelectronic device;

the second microelectronic device includes a first side and a second side opposite the first side;

the second pads comprise a plurality of second bond-pads on and/or in the first side of the second microelectronic device; and

the second conductive mating structures are coupled to corresponding second bond-pads on the first side of the second microelectronic device.

30. (Withdrawn) The set of stacked microelectronic devices of claim 25 wherein:

the first microelectronic device includes a first side, a second side opposite the first side, a first plurality of bond-pads on and/or in the first side, and a plurality of conductive links extending from the first side to the second side;

the conductive links have ends that define the first pads on the second side of the first microelectronic device;

the first conductive mating structures are coupled to corresponding first pads on the second side of the first microelectronic device;

the second microelectronic device includes a first side and a second side opposite the first side;

the second pads comprise a plurality of second bond-pads on and/or in the first side of the second microelectronic device; and

the second conductive mating structures are coupled to corresponding second bond-pads on the first side of the second microelectronic device.

31. (Withdrawn) The set of stacked microelectronic devices of claim 25 wherein the first conductive mating structures are formed on corresponding first pads and the second conductive mating structures are formed on corresponding second pads.

32. (Withdrawn) A set of stacked microelectronic devices, the set comprising:

a first microelectronic device including a first side, a second side opposite the first side, a plurality of bond-pads proximate to the first side, a plurality of conductive links coupled to corresponding bond-pads and extending from the first side to the second side, a plurality of first conductive mating structures aligned with corresponding conductive links on the second side, and a redistribution layer on the first side, the redistribution layer having a plurality of ball-pads electrically coupled to corresponding conductive links and/or bond-pads; and

a second microelectronic device including an integrated circuit, a plurality of first pads coupled to the integrated circuit, and a plurality of second conductive mating

structures at least proximate to corresponding first pads, wherein the second conductive mating structures project away from the second microelectronic device and have openings configured to receive and interface with corresponding first conductive mating structures of the first microelectronic device.

33. (Cancelled)

34. (Withdrawn) A set of stacked microelectronic devices, the set comprising:

a first microelectronic device including a first integrated circuit, a first side, a second side opposite the first side, a plurality of first bond-pads proximate to the first side and electrically coupled to the first integrated circuit, and a plurality of first conductive mating structures at least proximate to corresponding first bond-pads; and

a second microelectronic device including a second integrated circuit, a plurality of second bond-pads proximate to the first side and electrically coupled to the second integrated circuit, and a plurality of second conductive mating structures at least proximate to corresponding second bond-pads, wherein the second conductive mating structures project away from the second microelectronic device and have openings configured to receive and mate with corresponding first conductive mating structures of the first microelectronic device.

IX. EVIDENCE APPENDIX

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted.

X. RELATED PROCEEDINGS APPENDIX

No related proceedings are referenced in II. above, or copies of decisions in related proceedings are not provided.